Validation of an SEU Simulation Technique for a Complex Processor: PowerPC7400

Gary M. Swift[1], Sana Rezgui[2], Raoul Velazco[2]

[1]Jet Propulsion Laboratory
Radiation Effects Group
MS: 303-220, 4800 Oak Grove Dr.
Pasadena, CA 91109, USA

[2]TIMA Laboratory
46, Av. Félix Viallet
38031 Grenoble (France)

I. INTRODUCTION

[1]Published data on the processors sensitivities with respect to SEU is generally obtained from radiation ground testing during which the program executed by the DUT consists in the sequential inspection of each of the processor memory cells accessible to the user, through the execution of a suitable instruction sequence. In such programs, so-called static tests, typically considered memory cells are general-purpose registers, special registers (program counter, stack pointer...) and internal memory. Nevertheless, the register use and duty cycle of the final application will be very different, including using instructions not in the static tests and disturbing other potential SEU targets. The ideal would be the use of the final application program for radiation ground testing, but generally this program is either unknown or unavailable when the qualification testing is performed on candidate circuits to space projects.

To cope with this limitation, a *dynamic test strategy* can be applied. It consists in the execution, while exposing the studied architecture to radiation, of simple benchmark programs, supposed to be somewhat representative, and the observation of the produced results. The use of such benchmarks relies on the assumption that the SEU sensitive area is disturbed in a way not too different from the upset while running the flight application. Nevertheless, this strategy is still not relevant in case of a complicated flight experiment as is often the case.

Several fault injection techniques have been explored in order to predict the error rate of a studied processor running a given program by means of simulation techniques [1-2]. Among these techniques, the one we presented in [3], so-called CEU (Code Emulating an Upset) injection has been validated for different microprocessors. Its effectiveness was proved for different circuits by comparing radiation data and CEU based predictions [4-5]. The ultimate goal of this technique is to upset a bit in randomly selected sensitive memory cells of the DUT and to observe its consequences on the operation of the studied application. From iterated CEU injection experiments, can be derived the CEU error-ratios for the studied chip thus allowing the prediction of the application error rate without irradiating the processor while running the studied program.

In previous works, we have shown, by applying the CEU injection technique to different digital architectures based on several processors (the microprocessors 80C51 from Intel [3] and TS68332 [4] from Motorola and the digital signal processors TMS320C50 from Texas instruments and SHARC from Analog Devices [5]), that this approach has lead to excellent results. In fact, due to the large percentage of accessible zones by the instruction set (for example none of these processors contains cache memory) those results were somewhat expected. However, the CEU approach does not allow upset injection in targets, which cannot be read and written by means of the instruction set. This intrinsic limitation causes potentially a serious impact on the accuracy of the error rate prediction. To investigate this issue, we have performed experiments needed to predict the SEU application cross-sections for an architecture based on the PowerPC7400 microprocessor. The goal of this paper is thus twofold: to provide results on the sensitivity to radiation of the selected processor, the PowerPC7400, and to analyze the accuracy of error-rate predictions based on both the intrinsic SEU cross-section and results of the CEU fault injection, for a complex processor including instruction and data caches.

II. TESTING METHODOLOGY

The CEU methodology does not replace SEU testing, rather its purpose is to leverage the basic register susceptibility determined by static testing and predict the rate of visible errors and malfunctions from upsets of an arbitrary application program. This is accomplished by performing CEU injection on the chosen application. Details of how this works are

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discussed in this section and experimental results validating the methodology's effectiveness are in Section III.

A. *Error rate prediction methodology*

The main target of the CEU injection technique is to measure the CEU error-ratio for the studied chip running a given application. From both the underlying SEU cross-section, σ_{SEU} issued from ground testing and CEU error-ratio τ_{SEU} estimated from fault injection sessions for a particular application, can be derived σ_{SEU} *(application)*, which is the cross-section of a processor while running a particular program (equation1). In the following we will call it predicted *application cross-section.*

$$\sigma_{SEU}(application) = \tau_{SEU} \times \sigma_{SEU} \qquad (1)$$

The measured application cross-section can be obtained as the rate between the number of errors detected divided by the number of particles (integrated flux) while exposing the DUT to radiation (equation 2).

$$\sigma_{SEU}(application) = \frac{Number\ of\ errors}{Particle\ fluence} \qquad (2)$$

B. *Experimental set-up*

The hardware/software set-up needed to perform the required experiments (fault injection and radiation testing) was based on a dedicated system, the THESIC (Testbed for Harsh Environment Studies of Integrated Circuits) system, developed by TIMA laboratory [6]. The architecture of THESIC comprises:

- a motherboard, built around a microcontroller (the 87C52 from Intel), performing the following tasks: control all operation related with the DUT test (power on/off, current consumption control, test stimuli download, starting /stopping test cycles, receiving, pre-processing and transmitting data to/from user interface computer via the serial link (RS232).
- a daughterboard, designed and developed for each particular DUT for both ground testing and fault injection purposes.
- a computer, for user interface (on-line monitoring of test execution, displaying result in "understandable" format), and memory mass purposes (storing experiment history for later analysis).

A daughterboard has been built to support the PowerPC family where only the basic components necessary to run an application program were included. The Motorola PowerPC7400 (also know as G4) microprocessor is a low-power 32-bit implementation of the PowerPC Reduced Instruction Set Computer (RISC) architecture and contains a cache memory L1 (32K bytes) and a controller for an external cache memory L2 (1 Mbyte). It has a 3.3V I/O voltage and a 2.2V core voltage. The daughterboard clocks its input at 40 MHz and its processor core frequency is multiplied to 260 MHz. This last feature makes the execution of a small program running with the cache memory enabled 8 times faster than when the cache is disabled. This constitutes an additional particular and complex case is addressed by the CEU injection technique.

The PowerPC daughterboard includes SRAMs, EEPROMs memories (for data and program storage), the Memory Mapped Interface MMI (for the communications between the two boards), 5V compatible buffers (to provide an interface between the PPC7400 and the other memory devices), power supply regulators and a clock circuit. Two ALTERA FPGAs (EPM7128SLC84) have been added to implement the interface between the PowerPC7400 and the memory devices and to control the operation of the processor. FPGA1 is used to control the chip select signals, the MMI control signals, data transfer control, Reset and interrupt signals to the PowerPC7400. FPGA2 is used to control the address transfer and the write/read operations of the PowerPC7400 signals. The PowerPC7400 THESIC daughterboard block diagram is given in fig. 1.

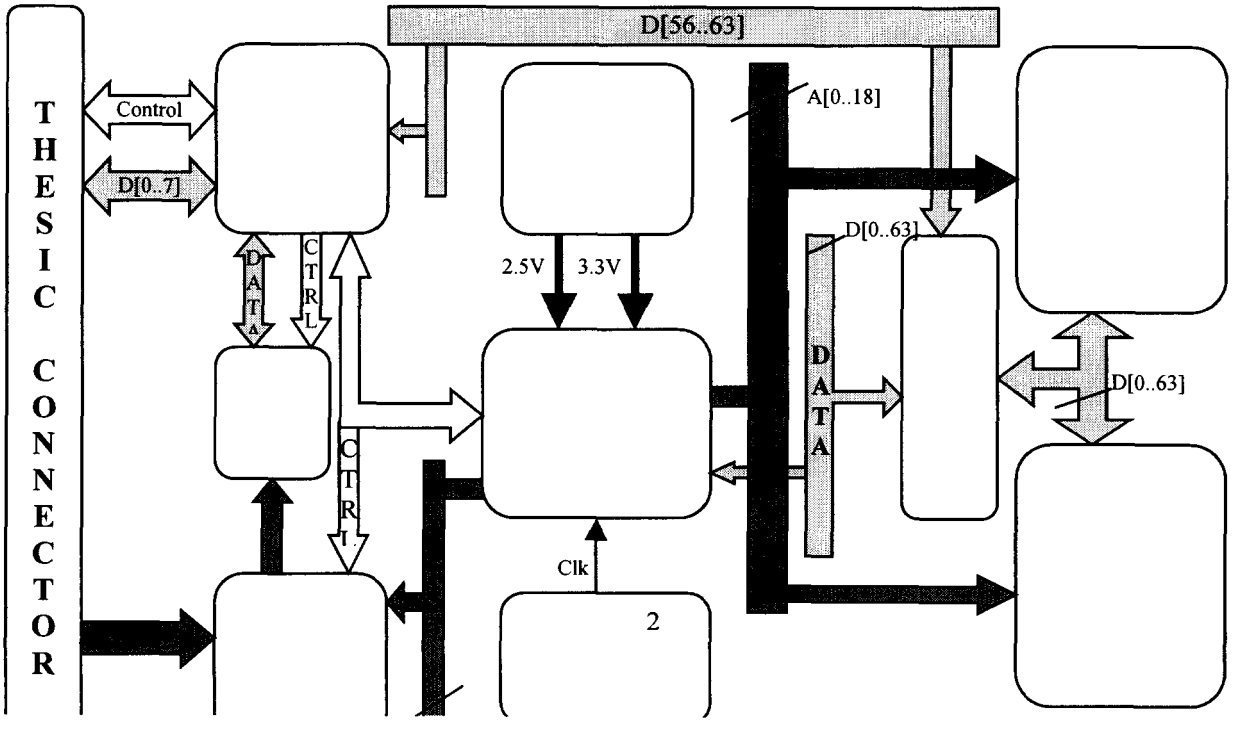


Figure 1: Block diagram of PPC 7400 THESIC daughterboard

III. EXPERIMENTAL RESULTS

As defined in the CEU injection methodology, the CEU targets include all the memory elements accessible by the instruction set. In the case of the PPC7400, the CEU targets set comprises only its internal registers excluding thus the huge SEU sensitive zone corresponding to L1 and L2 caches. Internal registers are General Purpose Registers (GPR), Floating Point Registers (FPR), Special Purpose Registers (SPR) and Altivec registers. The latter are not accessible by the instructions set of the PowerPC family and hence by the CEU injection technique. Consequently, bit flips are only injected in GPR, FPR and SPR registers, which are 55% of the PowerPC internal register bits (the Altivec's are the remaining 45%).

A. *Results of the CEU injection sessions*

CEU injection sessions have been performed on the sensitive zones of the PowerPC7400 running three benchmark programs (matrix multiplication, bubble sort and FFT). Only the FFT benchmark uses the floating point registers. Random CEU sessions were conducted in which 1000 faults were injected in accessible targets while running the benchmark programs for both PPC L1 cache configurations.

Provoked program errors were classified in three groups: tolerated faults, result errors, sequence loss. The first group, *tolerated faults*, corresponds to injected CEUs that had no effect on the known-good results. This occurs because of many memory elements whose content is not relevant for the rest of the program execution after the CEU occurs (for instance a register not used or a register which will be written after the bit flip occurrence, thus "erasing" the fault). Injected CEUs leading to *result errors* for which the expected results differ from those obtained for the correct program operation. Cases, where, after fault injection, no interrupt signal from the PowerPC was obtained, are classified in the *sequence loss* group.

Tables 1 and 2 summarize the obtained results. Note that for the Power PC, "Cache ON" means that both L1 Instruction and Data caches are enabled. As the accessible targets represent approximately 55% of the whole accessible area (excluding cache bits), the error rate predictions will thus be based on these percentages adjusted by the corresponding factor (55%) as shown in the fourth line of each table (in gray).

Table 1: CEU error rates with L1 Cache OFF

	Matrix	Bubble	F.F.T.
Tolerated faults	(97.3 ±6.23)%	(98.1 ±6.26)%	(95.8 ±6.19)%
Result errors	(1.8 ± 0.85)%	(0.4 ± 0.4)%	(2.7± 1.04)%
Sequence loss	(0.9 ± 0.6)%	(1.5 ± 0.75)%	(1.5 ± 0.75)%
CEU Error Rate	(2.7 ± 1.04)%	(1.9 ± 0.87)%	(4.2 ± 1.29)%
Effective CEU Error Rate	(1.35 ±0.73)%	(0.95 ± 0.61)%	(2.1 ±0.91)%

Table 2: CEU error rates with L1 Cache ON

	Matrix	Bubble	F.F.T.
Tolerated faults	(98.3 ± 6.27)%	(98.6 ±6.28)%	(97.6±6.25)%
Result errors	(0.4 ± 0.4)%	(0.5 ± 0.44)%	(0.5 ± 0.44)%
Sequence loss	(1.3 ± 0.72)%	(0.9 ± 0.6)%	(1.9 ± 0.87)%
CEU Error rate	(1.7 ± 0.82)%	(1.4 ± 0.75)%	(2.4 ± 0.98)%
Effective CEU Error rate	(0.85 ± 0.58)%	(0.7 ± 0.53)%	(1.2 ± 0.69)%

The main issue of these experiments is the percentage of injected CEUs, which result in observable program executions errors. Indeed, this figure combined with the measured register cross-sections will yield the predicted error rate for each studied application. For the selected benchmarks, the CEU rates are very low, between 0.7 % and 2.1 %. A rough estimation of the register usage is 20% for the matrix multiplication and the bubble sort programs, although the fraction of registers used is somewhat larger for the FFT application due to the use of floating point registers.

For the three benchmark programs, the number of detected errors when the L1 cache was OFF is significantly (around 50%) greater than when the cache is ON. Indeed, since the CEUs can only be injected in the internal registers and not in the cache memory, it was expected to obtain fewer result and sequence loss errors. Moreover, when the L1 cache is ON the operating frequency of the PPC becomes 8 times faster (260MHz). As the resolution of CEU occurrence instant (issued from an asynchronous interrupt generated from the Intel 87C52) equals 1 microsecond, the probability of missing sensitive instants will significantly increase. Compared to the result errors, the proportion of sequence loss errors is more important. This is likely due to the number of critical registers (Program Counter (PC), Linker Register (LR), Machine State Register (MSR), etc.) available in the PowerPC architecture.

B. *Radiation testing results*

In order to qualify the PowerPC7400 under heavy ion beams and to evaluate the effectiveness of the CEU injection technique, radiation testing campaign has been carried out 4-6 November 2001 at the Texas A&M cyclotron facility. For error rate estimation, the target of this study, the first step was to perform the register testing in which all the load/store registers were initialized with a pattern, prior inspecting their content to count upsets. The patterns used for 32 bits registers contained equal numbers of 0s and 1s (55AA00FF in hex), while for 64 bits registers this pattern was repeated.

Considering that while performing the static test the contents of the critical registers such as the Program Counter and the Machine State Register can not be set to arbitrary patterns (since they are variable) the portion of tested bits (accessible registers) in the PowerPC7400 processor is

approximately the half of the whole sensitive bits. To take into account this fact, all the obtained SEU cross-sections have been multiplied by two.

Table 3 summarizes the features of beam used, the breakdown of errors by category (upsets and sequence loss) and the underlying SEU cross section derived from this standard static test where the L1 cache has been disabled. This static test program involves only the registers accessible by the instructions set of the PowerPC family and the ones, which content is fixed during the execution of the test. Hence, only the half of the PPC internal registers (called tested bits in table 3) has been checked continually during the radiation testing. The derived results are given in the column 8 of the table 3 and the extrapolation of the device cross-section is shown in the column.

It can be concluded from the results given in table 3 and represented in the fig. 2 (according to the column 9 in table 3), that the SEU threshold is below 1.24 MeV/mg/cm2 and that a saturation cross section per device of 10^{-4} cm² is reached for a LET of approximately 10MeV/mg/cm2, which confirms the results obtained in [7]. In this reference, the authors apply static test strategies using a commercially available PowerPC7400 evaluation board (called Yellowknife).

Table 3: PPC G4 SEU Cross-sections (Cache OFF)

Heavy Ions	Effective LET (MeV/mg/cm²)	Energy (GeV)	Range (µm)	Fluence (Particles)	Upsets	Sequence loss errors	Cross-section (cm² / Tested bits)	Cross-section (cm² / device)
Neon	1.24	0.763	1525	$5.00\ 10^{7}$	3	3	$(1.2 \pm 0.97)\ 10^{-7}$	$(1.9 \pm 1.38)\ 10^{-7}$
Neon	2.28	0.348	403	$2.00\ 10^{7}$	2	36	$(1.9 \pm 0.62)\ 10^{-6}$	$(3.8 \pm 0.87)\ 10^{-6}$
Argon	4.04	1.48	948	$9.99\ 10^{6}$	52	2	$(5.4 \pm 1.47)\ 10^{-6}$	$(1.08 \pm 0.21)\ 10^{-5}$
Argon	9.3	0.442	149	$2.00\ 10^{7}$	957	58	$(5.07 \pm 0.31)\ 10^{-5}$	$(1.01 \pm 0.04)\ 10^{-4}$
Argon	13.2	0.215	58	$5.00\ 10^{7}$	5210	292	$(1.10 \pm 0.03)\ 10^{-4}$	$(2.2 \pm 0.04)\ 10^{-4}$
Krypton	15.8	2.668	491	$9.99\ 10^{6}$	682	52	$(7.34 \pm 0.54)\ 10^{-5}$	$(1.47 \pm 0.07)\ 10^{-4}$
Krypton	23.4	1.368	194	$1.00\ 10^{7}$	1384	65	$(1.45 \pm 0.08)\ 10^{-4}$	$(2.9 \pm 0.05)\ 10^{-4}$
Xenon	47.4	1.922	155	$9.98\ 10^{5}$	175	10	$(1.85 \pm 0.27)\ 10^{-4}$	$(3.7 \pm 0.38)\ 10^{-4}$

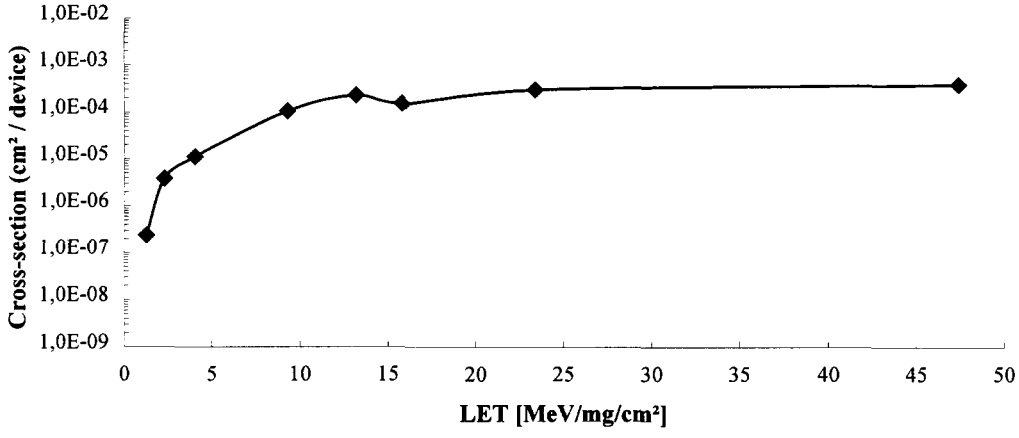


Figure 2: Underlying SEU cross-section of G4 PPC

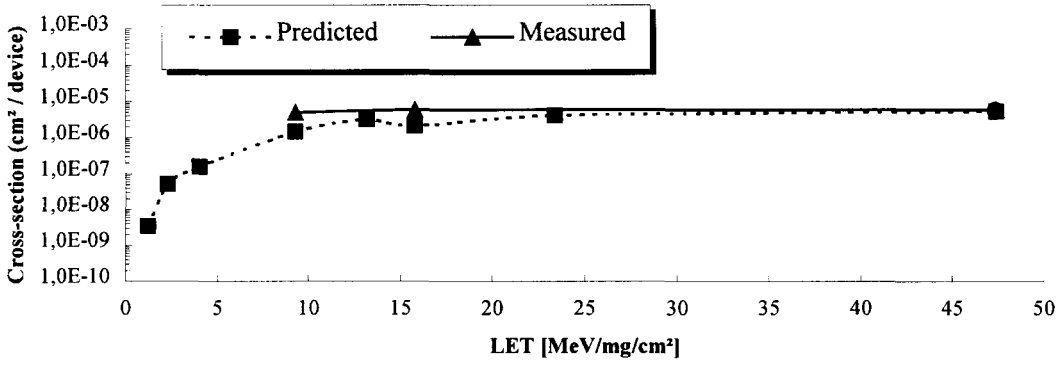
C. *Error rate estimation and comparison of predicted and measured error rates*

PowerPC7400 examples were exposed to the set of beams while running the benchmark programs in both L1 cache ON and cache OFF configurations. High fluxes were used, often having magnitudes of the order of 10^{5} particles/sec. Measured and predicted error rates (using equation 1) for each of the benchmark programs, are given in tables 4 and 5 and represented in figures 3 and 4. From these results, the sequence loss clearly appears as the main SEU error mode of the PPC. Indeed, compared with result errors, sequence losses are between 4 and 30 times more frequent. A general remark based on the analysis of these results is the low sensitivity to SEUs for all the exposed programs since the error cross-sections are not greater than 10^{-5} cm².

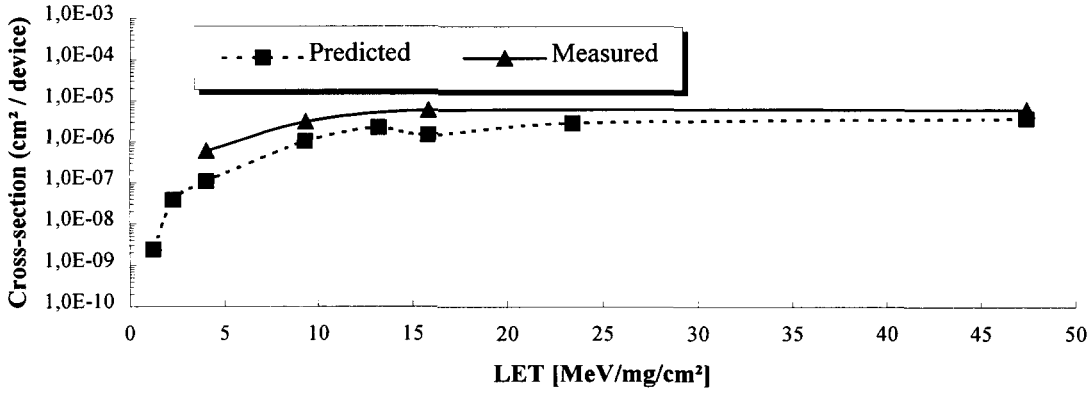
Table 4: Predicted and measured cross-sections for the PPC – G4, Cache OFF

Heavy Ions	Effective LET (MeV/mg/cm²)	Matrix Multiplication cross-section (cm² / device)	Bubble Sort cross-section (cm² / device)	FFT cross-section (cm² / device)

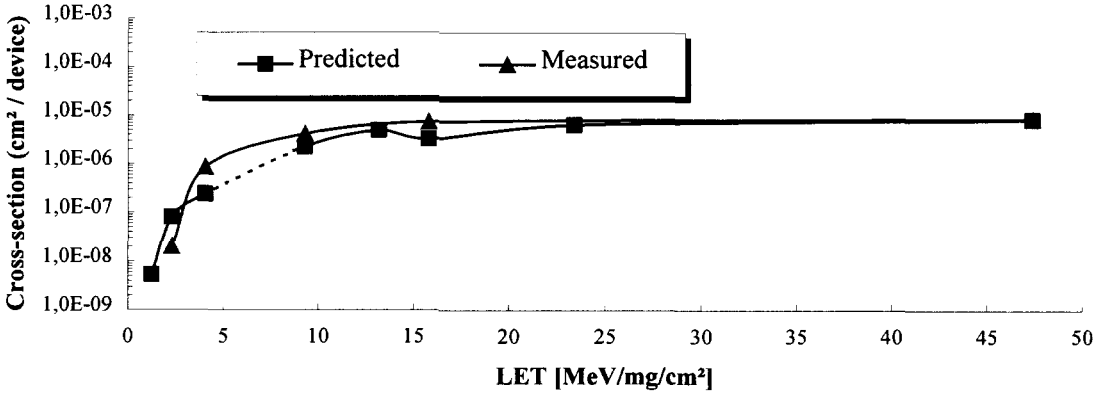
		Measured	Predicted	Measured	Predicted	Measured	Predicted
Neon	2.28		$(5.11 \pm 7.1)\ 10^{-8}$	$< 2\ 10^{-8}$	$(3.8 \pm 6)\ 10^{-8}$	$(2 \pm 4)\ 10^{-8}$	$(7.95 \pm 8.9)\ 10^{-8}$
Argon	4.04	$< 10^{-7}$	$(1.55 \pm 1.7)\ 10^{-7}$	$(6 \pm 4.89)\ 10^{-7}$	$(1.08 \pm 1.4)\ 10^{-7}$	$(3.8 \pm 1.74)\ 10^{-7}$	$(2.38 \pm 2.1)\ 10^{-7}$
Argon	9.3	$(4.96 \pm 0.63)\ 10^{-6}$	$(1.45 \pm 0.37)\ 10^{-6}$	$(3.06 \pm 0.49)\ 10^{-6}$	$(1.01 \pm 0.31)\ 10^{-6}$	$(5.17 \pm 1.44)\ 10^{-6}$	$(2.23 \pm 0.46)\ 10^{-6}$
Krypton	15.8	$(5.8 \pm 1.52)\ 10^{-6}$	$(2.09 \pm 0.63)\ 10^{-6}$	$(5.8 \pm 1.52)\ 10^{-6}$	$(1.47 \pm 0.52)\ 10^{-6}$	$(7.4 \pm 1.72)\ 10^{-6}$	$(3.25 \pm 0.78)\ 10^{-6}$
Xenon	47.4	$(5.8 \pm 1.52)\ 10^{-6}$	$(5.26 \pm 3.16)\ 10^{-6}$	$(6 \pm 1.57)\ 10^{-6}$	$(3.70 \pm 2.65)\ 10^{-6}$	$(8.41 \pm 0.21)\ 10^{-6}$	$(8.18 \pm 3.94)\ 10^{-6}$



a) for the matrix multiplication program with L1 cache OFF



b) for the bubble sort program with L1 cache OFF

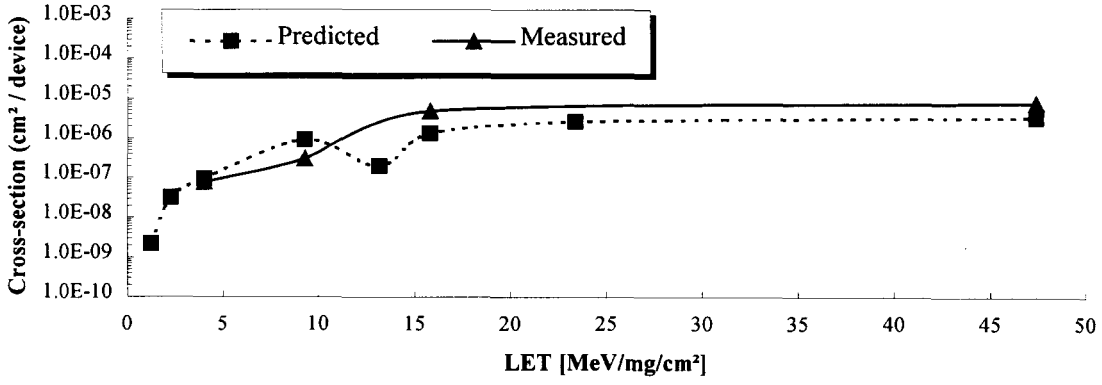


c) for the FFT program with L1 cache OFF

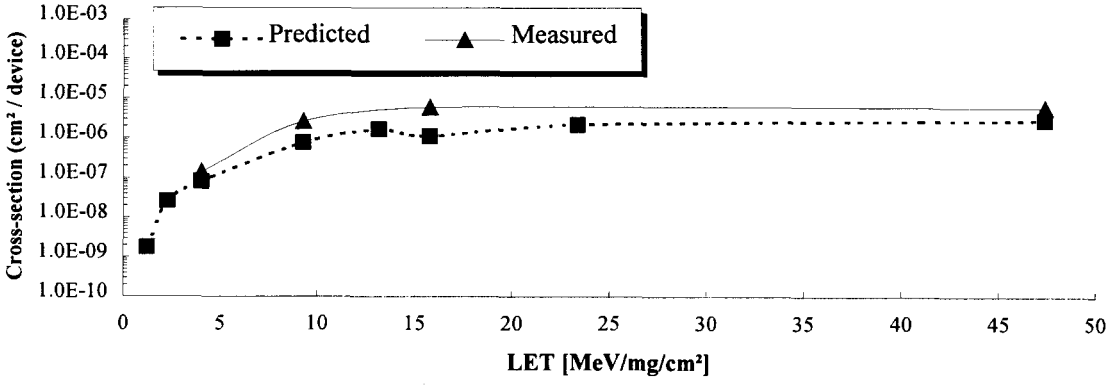
Figure 3: G4 PPC predicted and measured cross-sections to SEU for the three benchmarks programs with L1 Cache OFF

Table 5: Predicted and measured cross-sections for the PPC – G4, Cache ON

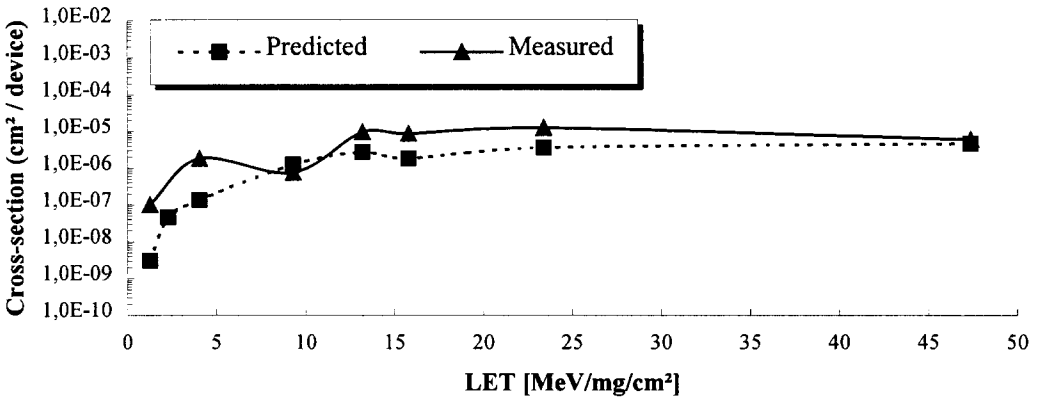
Heavy Ions	Effective LET [MeV/mg/cm²]	Matrix Multiplication cross-section (cm² / device)		Bubble Sort cross-section (cm² / device)		FFT cross-section (cm² / device)	
		Measured	**Predicted**	**Measured**	**Predicted**	**Measured**	**Predicted**
Argon	4.04	$(0.8 \pm 0.8)\ 10^{-7}$	$(0.96 \pm 1.35)\ 10^{-7}$	$(1.4 \pm 1.06)\ 10^{-7}$	$(7.95 \pm 1.23)\ 10^{-8}$	$(1.86 \pm 0.38)\ 10^{-6}$	$(1.36 \pm 1.61)\ 10^{-7}$
Argon	9.3	$(3 \pm 1.55)\ 10^{-7}$	$(9.03 \pm 2.93)\ 10^{-7}$	$(2.54 \pm 0.45)\ 10^{-6}$	$(7.44 \pm 2.66)\ 10^{-7}$	$(7.6 \pm 2.46)\ 10^{-7}$	$(1.27 \pm 0.55)\ 10^{-6}$
Argon	13.2		$(1.97 \pm 0.27)\ 10^{-6}$		$(1.62 \pm 0.25)\ 10^{-6}$	$(9.7 \pm 0.77)\ 10^{-6}$	$(2.77 \pm 0.32)\ 10^{-6}$
Krypton	15.8	$(4.8 \pm 1.38)\ 10^{-6}$	$(1.32 \pm 0.5)\ 10^{-6}$	$(5.8 \pm 1.52)\ 10^{-6}$	$(1.08 \pm 0.45)\ 10^{-6}$	$(8.9 \pm 1.88)\ 10^{-6}$	$(1.86 \pm 0.59)\ 10^{-6}$
Krypton	23.4		$(2.59 \pm 0.7)\ 10^{-6}$		$(2.13 \pm 0.63)\ 10^{-6}$	$(1.27 \pm 0.22)\ 10^{-5}$	$(3.66 \pm 0.81)\ 10^{-6}$
Xenon	47.4	$(7.7 \pm 1.75)\ 10^{-6}$	$(3.31 \pm 2.51)\ 10^{-6}$	$(5.8 \pm 1.52)\ 10^{-6}$	$(2.73 \pm 2.28)\ 10^{-6}$	$(6.07 \pm 1.28)\ 10^{-6}$	$(4.67 \pm 2.98)\ 10^{-6}$



a) for the matrix multiplication program with L1 cache ON



b) for the bubble sort program with L1 cache OFF



c) for the FFT program with L1 cache OFF

Figure 4: G4 PPC predicted and measured cross-sections to SEU for the three benchmarks programs with L1 Cache ON

As shown in table 4 and figure 3, the agreement is fairly good between predictions and measurements derived from the experiments performed with the benchmark programs where the L1 cache is disabled. For the L1 cache enabled, results shown in table 5 and given in figure 4, even worst predictions are still within an order of magnitude. Indeed, if error uncertainties are considered, predictions and measures are within the same interval. This achievement is more particularly remarkable according to the large number of sequence loss errors, which as stated before, cannot be simulated by the CEU injection approach in an accurate way. In addition, although a higher SEU sensitivity when enabling the cache was expected, the results show that the sensitivities of all of the three benchmark programs are approximately the same in both cache configurations. Such an unexpected result may come from the short cache duty cycle due to the high operating frequency of the PowerPC when enabling the cache (260 MHz), which makes the registers duty cycles remain approximately the same in both cache configurations.

Exception occurrence (illegal instruction, floating point unavailable, data alignment...) was observed many times during radiation testing. Upsets causing exceptions may result either in tolerated faults or result errors or sequence-loss errors. The latter case indicate errors in critical control registers (for instance in the Hardware Implementation-Dependent register 0 (HID0)) or in processor's control parts which are not accessible by means of the instruction set and thus by the CEU injection technique. The breakdown of the loss sequence errors detected by the exceptions occurrence and this for the three benchmark programs are given in tables 6 and 7 for both configurations cache OFF and cache ON.

The high rate of exception occurrence during radiation testing shows that a significant amount of sequence-loss errors may be recovered by suitable exception handling programs. From the analysis of the results, it can be shown that, for the cache OFF configuration, the percentage of sequence loss errors detectable by exception can be more than 50%. For the cache ON configuration, in the best case (for bubble sort program), this percentage can reach 20%. Note that, for a given program and cache configuration, the analysis of exception detection for all the beams shows that the ratio of sequence loss errors detectable by exception is approximately the same for all the beams.

Table 6: Sequence loss errors detected by exceptions under Argon heavy ion beams for... Effective LET = 9.3 MeV/mg/cm, Cache OFF

Exceptions	Bubble	Matrix	FFT
SR: 0x100		2	
MC: 0x200		1	2
DSI: 0x300			
ISI: 0x400	2	1	
Align.: 0x600	2	1	
Ill. In: 0x700	14	17	8
UFP: 0x800	2	12	
Dec.: 0x900			
Trace: 0xD00			1
PM:0xF00	1		
TMI: 0x1700			
Total of sequence loss errors detected by exceptions	21	34	11
Total of sequence loss errors detected by THESIC watch dog	54	56	53

Table 7: Sequence loss errors detected by exceptions under Argon heavy ion beams for... Effective LET = 9.3 MeV/mg/cm, Cache ON

Exceptions	Bubble	Matrix	FFT
SR: 0x100			
MC: 0x200			1

DSI: 0x300 ISI: 0x400 Align.: 0x600 Ill. In: 0x700 UFP: 0x800 Dec.: 0x900 Trace: 0xD00 PM:0xF00 TMI: 0x1700	17 7	1	2
Total of sequence loss errors detected by exceptions	24	1	3
Total of sequence loss errors detected by THESIC watch dog	121	14	26

IV. Conclusion and Future Work

This paper presents the results of performing fault injection and radiation testing using the THESIC PowerPC daughterboard. The underlying register cross-section and the benchmark cross-sections were obtained from radiation testing at Texas A&M cyclotron facility. CEU fault injection did not cause particular difficulties to be implemented for the register set of Power PC, but CEUs could not be injected in the internal cache memories.

Predicted error rates for benchmark programs were derived according to the CEU injection methodology. For both cache configurations, the predictions were in good agreement with the measurements despite the contribution of the control part targets, which are not accessible to CEUs. This successful result can be explained by the fact that although the execution flow of programs in cache ON and cache OFF modes is very different, the registers duty cycles remain the same due to the short cache duty cycle. The incidence of cache configuration is thus negligible, at least for the programs used in this study. These experiments bring new evidence of the effectiveness of the error rate prediction approach based on the CEU injection technique.

V. Acknowledgements

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